REMARKS

Claims 1-5, and 7 are now pending in the application. Claims 6 and 8 are cancelled. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 102

Claims 1 and 7 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Hidaka et al. (U.S. Pat. No. 6,933,915). This rejection is respectfully traversed.

Claim 1 recites a semiconductor integrated circuit comprising a memory cell, a write/read circuit, a read circuit, a CPU-system control circuit, a timing generator circuit, and a display-system control circuit. The timing generator circuit generates a display-data read request signal. The CPU-system control circuit controls the write/read circuit so that a data write or read operation based on at least one of a write request and a read request from a CPU is performed for a first period. The display-system control circuit controls the read circuit by generating a display-data read control signal based on at least one of a write request signal and a read request signal received from the CPU and the display-data read request signal so that data to be supplied to a display panel is read for second period which does not overlap the first period.

Hidaka et al. fails to teach or suggest the integrated circuit recited by claim 1. In Hidaka et al., the CPU sends an I/F signal when it has access to a display-data RAM. Hidaka et al. Col. 4, lines 62-63. When the CPU does not have access to the display-data RAM, data is sent to a liquid crystal display. Hidaka et al., Col. 5, lines 13-15.

In the integrated circuit recited by claim 1, however, the CPU-system control circuit controls the write/read circuit based on at least one of the write request and the read request from the CPU. The display-system control circuit controls the read circuit by generating the display-data read control signal based on at least one of the write request and the read request received from the CPU and the display-data read request signal. Data to be supplied to the display panel is read for a second period which does not overlap a first period. Access control in the manner recited by claim 1 is distinguishable from the Hidaka et al. system, which uses the single I/F signal when the CPU has access to the display-data RAM. Thus, Hidaka et al. does not teach or suggest the integrated circuit recited by claim 1.

Therefore, claim 1 defines over the prior art and reconsideration and withdrawal of the rejection are respectfully requested. With regard to claim 7, Applicant notes that claim 7 depends from claim 1, which defines over the prior art as discussed above. Therefore, claim 7 also defines over the prior art and reconsideration and withdrawal of the rejection are respectfully requested.

ALLOWABLE SUBJECT MATTER

The Examiner states that claims 2-5 would be allowable if rewritten in independent form. Accordingly, Applicant has amended claim 2 to include the limitations of the base claim. Claims 3-5 each depend from claim 2. Therefore, claims 2-5 should now be in condition for allowance.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: April 21, 2006

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